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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of : Vladislav Vashchenko

Serial No.: 09/944,426 — Examiner: Ori Nadav

Filed: 8/30/2001 — Art Unit: 2811

For: HIGH HOLDING VOLTAGE LVTSCR-LIKE STRUCTURE

APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Dear Sir:

The Appellants hereby submit this Brief in triplicate in support of their appeal from a final rejection by the Examiner, mailed April 17, 2003 and follow-up Advisory Action mailed August 8, 2003, in the above case. The Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above patent application.

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I. REAL PARTY IN INTEREST

The real party in interest is National Semiconductor Corporation, a corporation of Delaware having a principle place of business at 2900 Semiconductor Drive, M/S D3-579, Santa Clara, CA 95051

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences

III. STATUS OF THE CLAIMS

Claims 1-6 are currently pending. Claim 1 is withdrawn from consideration and is not being appealed.

IV. STATUS OF AMENDMENTS

No after final amendment was made.

V. SUMMARY OF INVENTION

The invention relates to a LVTSCR-like structure for electrostatic discharge (ESD) protection, which has a higher holding voltage than a prior art LVTSCR, by including additional p and n regions in a p-well, to define at least one forward biased p-n junction in the p-well.

VI. ISSUES

The issue is whether the prior art cited, namely Ham, discloses a structure having a p-n junction in the p-well that is forward biased during normal operation.

VII. GROUPING OF CLAIMS

Claims 2-6 were rejected based on the common argument that Ham anticipates the invention defined in the claims.

VIII. ARGUMENT

Summary of arguments:

Claims 2-6 were rejected under 35 USC 102(b) in view of Ham.

The examiner argues that Ham teaches in figure 7 a method that includes providing a p-n junction diode 40,42 in the p-well that is forward biased during normal operation.

It is respectfully submitted that there is no forward biased p-n junction anywhere in Ham. In fact the only biased junctions are the following:

a) The p-well/n-well junction, which is reverse biased (n-well connected to VDD and p-well connected to VSS).

b) A reverse biased junction between p+ region 48 (tied to I/O pad) and n-well (tied to the higher voltage VDD). This is described in column 4, lines 59-67 and shown in Figure 8 as reverse biased diode 56.

c) A reverse biased diode between the p-well (tied to VSS) and n+ region 44 (tied to the I/O pad). This is shown in Figure 8 as reverse biased diode 54).

(The regions 40, 42 are both tied to VSS and therefore the p-n junctions across these two regions is not biased. Similarly the regions 50, 52 are both tied to VDD and therefore the junction between them is also not biased.)

Thus, Ham has no forward biased junctions.

In contrast to Ham, the present application has two p-n junctions in the p-well, namely (p+ region 420/n+ region 422) and (p+ region 424/n+ region 426) (see page 5, lines 36-38). The electric field across the structure between drain 406, 408 and source, biases the two diodes in a forward direction to provide the additional current path when they break down at approximately 1V (see page 6, lines 12-14).

The examiner argues that Vdd can be positive or negative and refers to column 4, lines 59-62. There is no such support in the cited section of Ham.

The examiner also argues that the limitation of a forward biased p-n junction is not recited in the claims. However the amendment filed February 10, 2003 clearly includes this limitation. In the case of claim 3 it is stated that the current path is from anode to cathode, which is also not disclosed in Ham.

Since Claims 2-6 are distinguishable over the prior art, allowance of the claims 2-6 is respectfully requested.

Charge Our Deposit Account

If there are any further charges not accounted for herein, please charge them to our deposit account No. 140448

Respectfully submitted,

Vollrath & Associates

Date: 5/16/, 2003

Jurgen K. Vollrath
Reg. No. 49,098
Attorney for Appellants

IX. APPENDIX

2. A method of increasing the holding voltage of a LVTSCR structure, comprising forming at least one additional p-region and n-region inside a p-well of the structure to define a p-n junction that is forward biased during normal operation.

3. A method of increasing the holding voltage of a LVTSCR-like structure having an anode and a cathode, comprising providing an alternative current path from anode to cathode through a p-well of the structure, other than purely the current path from anode to cathode through the p-material of the p-well.

4. A method of claim 3, wherein the alternative current path defines a lower resistance current path than the p-well.

5. A method of claim 4, wherein the lower resistance current path takes the form of at least one p-n junction that is forward biased under normal operating conditions, formed in the p-well.

6. A method of claim 4, wherein at least one diode is formed in the p-well which provides a low resistance current path once the voltage across the at least one diode is exceeded.